(A tentative program which will be updated every week)

2022 IEEE Silicon Nanoelectronics Workshop

Hilton Hawaiian Village, Honolulu, HI USA

June 11-12, 2022

Technical Program (Hybrid Event)

Opening Remarks

Saturday June 11 13:00

Steve Chung, NYCU

Session 1: Plenary I

Saturday June 11 13:10

Session Chair: Pei-Wen Li, National Yang Ming Chiao Tung University

13:10 – 13:50 **1.1 (Plenary) 3D MOSAIC: MOnolithic/Stacked/Assembled IC**, *Philip Wong, Stanford University*

Session 2: Ferroelectric & TMD Electronics

Session Chair: TBA

13:55 – 14:20 **2.1 (Invited) Hafnium-based FeRAM for Next-generation High-speed and High-Density Embedded Memory**, *S.-C. Chang, U. E Avci, Intel Corp.*

14:20 – 14:45 **2.2 (Invited) Mechanism of HfO_2-FeFET Memory Operation Revealed by Quantitative Analysis of Spontaneous Polarization and Trap Charge**, *R. Ichihara, Y. Higashi, K. Suzuki, H. Kusai, Y. Yoshimura, T. Hamai, Y. Kamiya, K. Takahashi, K. Matsuo, Y. Nakasaki, H. Miyagawa, M. Suzuki, K. Sakuma, Y. Kamimuta, M. Saitoh, Kioxia Corp.*

14:45 – 15:10 **2.3 (Invited) Perspective of Ferroelectric-HfO_2 Materials for Electron Device Applications**, *S. Migita, National Institute of Advanced Industrial Science and Technology (AIST)*

15:10-15:25 **2.4 A Vertical Channel Ferroelectric/Anti-Ferroelectric FET with ALD InOx and Field-Induced Polar-Axis Alignment for 3D High-Density Memory**, *Z. Li[1], J. Wu[1], X.*

Mei[1], X. Huang[1], T. Saraya[1], T. Hiramoto[1], T. Takahashi[2], M. Uenuma[2], Y. Uraoka[2], M. Kobayashi[1], [1]The University of Tokyo, [2]Nara Institute of Science and Technology

15:25-15:40 **2.5 Suppressing Interfacial Layer Degradation in $Hf_{0.5}Zr_{0.5}O_2$-based FeFETs Using a Pre-erase Strategy during Program/Erase Cycling**, *G. Zhao[1], W. Wei[1], L. Tai[1], M. Tang[1], X. Li[1], H. Xu[2], J. Chai[2], X. Wang[2], J. Wu[1], X. Zhan[1], J. Chen[1], [1]Shandong University, [2]Institute of Microelectronics of Chinese Academy of Sciences*

15:40-15:55 **2.6 Wafer scale integration of MX_2 based NMOS Only Ring Oscillators on 300 mm Wafers**, *T. Schram, H. Celiker, Q. Smets, I. Asselbergs, G. S. Kar, K. Myny, imec*

Coffee Break 15:55-16:20

Session 3: Advanced Computing

Session Chair: TBA

16:20-16:45 **3.1 (Invited) Silicon-based Quantum Computing: Scaling Strategies**, *M. Fernando Gonzalez-Zalba1, Quantum Motion Technologies*

16:45-17:10 **3.2 (Invited) Some Benefits of CMOS Nanowire Devices for Spin Quantum Bits,** *R. Ezzouch, N. Piot, M. Bassi, C. Yu, B. Brun-Barrière, S. Zihlmann, V. Schmitt, V. Michal, J. Abadillo-Uriel, Y. -M. Niquet, H. Niebojewski, B. Bertrand, M. Vinet, R. Maurand, Xavi er Jehl, S. De Franceschi Univ. Grenoble Alpes CEA-Leti*

17:10-17:25 **3.3 Importance of Stochastic Components for Ising Hamiltonian-based Invertible logic**, *L. Hutin[1], P. Talatchian[2], P. Ilha Vaz[2], A. Sidi El Valli[2], A. Bazzi[1], N.-T. Phan[2], F. Andrieu[1] [1]CEA-Leti Minatec, [2]SPINTEC, Univ. Grenoble Alpes / CEA / CNRS*

17:25-17:40 **3.4 Barrier and Self-aligned Electrode Engineering in Self-assembled Ge Quantum-dots Array for CMOS Integratable Quantum Electronic Devices**, *I-H. Wang, T. Tsai, Y.-J. Chiu, H. -C. Lin, P. W. Li, National Yang Ming Chiao Tung University*

17:40-17:55 **3.5 Evaluation of Single-Electron Tunneling Operation in High-Concentration Codoped Si Nano-Transistors,** *T. Kaneko, T. T. Jupalli, D. Moraru, Shizuoka University*

17:55-18:10 **3.6 Computation-in-Memory with Hybrid Integration of Non-Volatile Memory & SRAM for Reservoir Computing,** *S. Koshino, C. Matsui, K. Takeuchi, The University of Tokyo*

Session 4: Plenary II

Sunday June 12 08:30 a.m.

Session Chair: TBA

08:30-09:10 **4.1 (Plenary) Extremely-Thin Channel FET Technology for Advanced Logic CMOS**, *S. Takagi, K. Sumita, C. T. Chen, X. Han, K. Toprasertpong, M. Takenaka, The University of Tokyo*

Session 5: Advanced Transistors

Sunday June 12 09:10 a.m.

Session Chair: TBA

09:10-09:35 **5.1 (Invited) Cryogenic Steep Slope Field-Effect Transistors**, *J. Knoch[1], B. Richstein[1], Y. Han[2], D. Konig [3], M. Frentzen[1], L. Hellmich[1], J. Klos[1], S. Scholz[1], Q.T. Zhao[2], [1]RWTH Aachen University, [2]Peter Grunberg Institute (PGI-9), [3]University of New South Wales*

09:35-09:50 **5.2 Improved Characteristics of Ge CMOS Devices by Low Temperature Supercritical Fluid Treatment**, *D.-B. Ruan, K.-S. Chang-Liao, National Tsing Hua University*

09:50-10:05 **5.3 A Built-in Spice Time-domain Variation Model of the BTI-induced Random Trap Fluctuation (RTF) in 14 nm FinFETs**, *L. C. Lin[1], Z. Y. Wang[2], M. Y. Lee[1], J. K. Chang[1], E. R. Hsieh[2], J. C. Guo[1], S. S. Chung[1], [1]National Yang Ming Chiao Tung University, [2]National Central University*

10:05-10:20 **5.4 Effect of Bit Line Voltage Stress on Half-Selected Device in 1T1R Array**, *J. Lai[1,2], D. Dong[2], X. Zheng[2], J. Yu[2], W. Sun[2], X. Xu[2], [1]University of Science and Technology of China, [2]Chinese Academy of Sciences*

10:20-10:35 **5.5 V_{DD} Scalability of Complementary Ternary Stack Channel Transistor,** *K. Kim, S.-Y. Kim, Y. Lee, H.-W. Lee, H. Kwon, H. I Lee, B. H. Lee, Pohang University of Science and Technology (POSTECH)*

10:35-10:50 **5.6 Low-Frequency Noise Characteristics of BEOL-Compatible IWO Transistor**, *Y.-C. Luo[1], H. Ye[2], W.Chakraborty[2], J. Hur[1], P. V. Ravindran[1], A. I. Khan[1], S. Datta[2], S. Yu[1], [1]Georgia Institute of Technology, [2]University of Notre Dame*

Coffee Break 10:50-11:10

Session 6: Silicon Photonics

Sunday June 12 11:10 a.m.

Session Chair: TBA

11:10-11:35 **6.1 (Invited) Nano-SOI Photodetectors for High Sensitivity and Unique Functionality**, *H. Inokawa[1], H. Satoh, A. Nagarajan, R. Manivannan, D. Elamaran, Shizuoka University*

11:35-11:50 **6.2 Embedded Tensile-strained Ge Quantum-dots in Si_3N_4/SiO_2 Microdisk resonators array for light emitters**, *C. H. Lin, P. W. Li, National Yang Ming Chiao Tung University*

11:50-12:05 **6.3 Silicon Quantum Dots with Large Stokes Shift and Long Photoluminescence Lifetime for Energy and Biomedical Applications**, *C. C. Tu[1,2], S. Han[2], G. Chen[2], W. Yang[2], H. C. Kuo, [1]Hon Hai Research Institute, [2]Shanghai Jiao Tong University*

Lunch Break 12:05-13:20

Session 7: Poster

Sunday June 12, 13:20 – 15:20

13:20 **Poster** (oral introduction, 2 minutes each)

Session Co-Chairs: TBA

P1-1 **Simulation and Investigation of 2D FeFET Synapse with Identical Pulse Scheme for Neuromorphic Applications**, *Y. J. Hsu, Y. C. Luo, Y. C. Chen, C. L. Fan, P. Su, National Yang Ming Chiao Tung University*

P1-2 **Forming, Compliance Free Operation in Al2O3/TiOx Based RRAM Array Using Naturally Generated AlO_x Interlayer**, *S. Kim[1], T. H. Kim[1], K. Hong[1], H. Kim[2], B. G. Park[1], [1]Seoul National University, [2]Inha University*

P1-3 **Inelastic Cotunneling in the Coulomb-Blockade Transport in Donor-Atom Transistors**, *P. Yadav[1], S. Chakraborty[1], D. Moraru[2], A. Samanta[1], [1]Indian Institute of Technology Roorkee, [2]Shizuoka University*

P1-4 **Integrated Synaptic Phototransistors Mimicking Neural Population Coding,** *Y. Wang, M. Bu, H. Lu, Y. Zheng, D. Yang, X. Pi, Zhejiang University*

P1-5 **Optimal Read Voltages of Retention-after-Cycling in Triple-level-cell (TLC) 3D NAND Flash Memory and its High-precision Modeling Method**, *H. Lin, Y. Guo, Y. Xi, Y. Kong, X. Zhan, J. Chen, Shandong University*

P1-6 **Investigation of Memory Non-Ideality Impacts on Non-Volatile Memory Based Computation-in-Memory AI Inference by Comprehensive Simulation Platform**, *K. Higuchi, C. Matsui, K. Takeuchi, The University of Tokyo*

P1-7 **Investigation of Interlayer Surface Roughness induced Variation in Scaled 2D Ferroelectric-FET Nonvolatile Memories,** *L. E. Chang, Y. S. Liu, P. Su, National Yang Ming Chiao Tung University*

P1-8 **Multi-synaptic conductance control using conductive polymer wiring,** *N. Hagiwara[1], T. Asai[1], M. Akai-Kasaya[1,2], [1]Hokkaido University, [2]Osaka University*

P1-9 **A Novel Design of Overpass Channel Synapse Array for Neuromorphic System**, *T. Jang, J. Bosung, K. Park, S. Song, B.G. Park, Seoul National University*

P1-10 **Coulomb Blockade Oscillations Observed in Micrometer-sized Single-Electron Device of Metal Nanodot Array**, *T. Gyakushi, I. Amano, A. Tsurumaki-Fukuchi, M. Arita, Y. Takahashi, Hokkaido University*

P1-11 **RF Reflectometry of NEMS Motional Capacitance with Micromanipulator Probe**, *R. Celis-Cordova, E. M. Williams, G. J. Quintero Cayaspo, J. J. Gose, A. F. Brown, J. D. Chisum, A. O. Orlov, G. L. Snider, University of Notre Dame*

P1-12 **Dynamic Single-Electron Transistor Model with Capacitance Analysis Capability**, *A. Singh, T. Nishimura, H. Satoh, H. Inokawa, Shizuoka University*

P1-13 **Realization of Dendritic characteristics Based on Metal Oxide Resistive Switching Memory**, *Y. Yi, X. Ding, S. Song, Y. Feng, L. Liu, Peking University*

P1-14 **Fully CMOS integrated programmable charge-to-digital readout operating at cryogenic temperature for semiconductor qubits**, *M. Castriotta[1], G. Guiducci[1], E. Prati[2,3], G. Ferrari[1], [1]Politecnico di Milano, [2]Consiglio Nazionale delle Ricerche, [3]Università degli Studi di Milano*

P1-15 **Investigation of Coupling Effect on Capacitor-based Neural Network**, *J. Yu[1], S. Hwang[1], H. Kim[2], B. G. Park[1], [1]Seoul National University, [2]Inha University*

P1-16 **Comparative Analysis of Vertically Stacked Nanosheet FET based SONOS Memory**, *Md. Hasan Raza Ansari, N. El-Atab, King Abdullah University of Science and Technology (KAUST)*

P1-17 **Analog-Digital Hybrid Neuron with Up/Down Counter for Neuromorphic System**, *Y. Kim, B. Jeon, K. Park, B. G. Park, Seoul National University*

P1-18 **Investigation of Poly-Si TFT Based U-shaped Channel Synaptic Device,** *D. Ryu, Y. Kim, T. Jang, S. Song, B. Jeon, B. G. Park, Seoul National University*

P1-19 **Deposition and characterization of low-density carbon nanotube networks on CMOS-compatible platform**, *R. S. Singh, K. Takagi, T. Aoki, J. Moon, Y. Neo, F. Iwata, H. Mimura, D. Moraru, Shizuoka University*

P1-20 **Design of Single-Electron Reservoir Computing Circuit and Evaluation of Its Learning Function**, *S. Watanabe, T. Oya, Yokohama National University*

P1-21 **Impact of Double HZO on Ferroelectric FinFET and 1T Memory Application**, *Y. F. Chung, S. T. Chang, National Chung Hsing University*

P1-22 **Hysteresis-free Behavior and Improved Performance of Negative Capacitance Optimized Bulk MOSFET,** *H. Kansal, A. S. Medury, Indian Institute of Science Education and Research*

P1-23 **Dual-Mode GaN MOS-HEMT of Cascode Configuration with Si Ferroelectric Hf1-xZrxO_2 FET,** *C.-Y. Liao[1], K.-Y. Hsiang[1,2], Z.-F. Lou[1], C.-Y. Lin[1], W.-C. Ray[1], F.-S. Chang[1], C.-C. Wang[1], Z.-X. Li[1], H.-C. Tseng[1], J.-Y. Lee[1], P.-H. Chen[1], J.-H. Tsai[1], P.-G. Chen[1], M. H. Lee[1], [1]National Taiwan Normal University, [2]National Yang Ming Chiao Tung University*

Session 8: Computing in Memory

Sun June 12 15:20

Session Chair: TBA

15:20-15:45 **8.1 (Invited) Study of Analog Weights Based Computing-in-Memory (CIM) using a Highly Reliable and Small-Noise Vertical-Channel Gate-All-Around Split-Gate Floating Gate NOR Flash for Vector Matrix Multiplication (VMM) Accelerator**, *H.-T. Lue, C.-H. Fu, T.-H. Hsu, M.-L. Wei, T.-H. Yeh, K.-C. Wang, C.-Y. Lu, Macronix International Corp.*

15:45-16:00 **8.2 Compact CiM Co-optimized by Heterogeneous Multi-level ReRAM &**

Random Weight SNN for Event-based Vision Sensor of Edge AI, *S. Koshino, N. Misawa, C. Matsui, K. Takeuchi, The University of Tokyo*

16:00-16:15 **8.3 A $4F^2$ Vertical Gate-all-around Nanowire Compute-in-memory Device Integrated in (1T1R) Cross-Point Arrays on Silicon,** *M. S. Ram, K.-M. Persson, Lars-Erik Wernersson, Lund University*

16:15-16:30 **8.4 Accurate and Stable SNN Inference Management System with Pulse Synchronization and Transfer Control Modules**, *S. Song, B. Jeon, T. Jang, D. Ryu, B.-G. Park, Seoul National University*

16:30-16:45 **8.5 Linear and Symmetric Weight Update of $CuO_x/HfO_x/WO_x$ ECRAM Synapse for Neuromorphic Systems**, *H. Kang, H. W. Kim, E. Hong, N. Kim, J. Woo, Kyungpook National University*

16:45-17:00 **8.6 Machine Learning Assisted Nanoscale Device Modeling for Nanosheet FETs with Process Variations**, *Y. Lyu, W. Chen, M. Zheng, B. Yin, J. Li, L. Cai, Sun Yat-Sen University*

Closing Remarks